layer is formed, which is comprised of a resist resin of the positive type as similar to that according to Example 1-2, and then a patterning for a recess part thereof is performed therewith. Further, regarding the MOSFET according to Comparative example 3, the point is different therefrom that a mask layer is formed, which is comprised of SiO_2 as similar to that according to Comparative example 1, and then a patterning for a recess part thereof is performed therewith. Still further, an on-resistance and a breakdown voltage thereof are measured for each of the MOSFETs according to Example 3-1, 3-2 and Comparative example 3 respectively. Furthermore, each of angles are measured respectively, for which each of the side walls is standing up regarding each of inclining formation layers respectively.

[0068] FIG. **10** is a chart showing an angle at a standing up thereof, an on-resistance and a breakdown voltage for each of the MOSFETs according to Example 3-1, 3-2 and Comparative example 3 respectively. As shown in FIG. **10**, in the case of Comparative example 3, the on-resistance is high as 16 mΩ cm^2, and the breakdown voltage is low as 200 V. On the contrary, in the case of Example 3-1 and 3-2, each of the on-resistances is lower as 5 mΩ cm^2 and 9 mΩ cm^2 respectively. Moreover, each of the breakdown voltages is higher as 530 V and 550 V respectively, that are the values as approximately similar to the value of the breakdown voltage as 600 V, which is estimated with using the thickness of the drift layer. That is to say, it becomes able to confirm that there becomes no localized convergence of the electric field occurring at between the gate and the drain regarding the MOSFETs according to Example 3-1 and 3-2.

[0069] Here, according to the above described first and the second embodiment, regarding the side wall of the semiconductor operating layer, the angle corresponding to the surface of the lower part semiconductor layer is similar in both directions thereof. However, an angle may be different between for example, for a part at a carrier drifting layer and for a part at a carrier supplying layer. Moreover, it may be not a straight shape but be curved as well. Ditto regarding the carrier drifting layer and the carrier supplying layer according to the third embodiment. Furthermore, according to the above described third embodiment, the MOSFET is the n type in which the carrier is an electron, however, the present invention is not limited thereto, and it is able to apply to an MOSFET of p type as well.

[0070] Although the invention has been described with respect to specific embodiments for a complete and clear disclosure, appended claims are not to be thus limited but are to be construed as embodying all modifications and alternative constructions that may occur to one skilled in the art that fairly fall within the basic teaching herein set forth.

What is claimed is:

1. A field effect transistor comprising:
- a substrate;
- a semiconductor operating layer having a recess part and formed on the substrate;
- an insulating layer formed on the semiconductor operating layer including the recess part;
- a gate electrode formed on the insulating layer at the recess part; and
- a source electrode and a drain electrode formed on the semiconductor operating layer with the recess part in between and electrically connected to the semiconductor operating layer,
- wherein said recess part includes a side wall protruding and inclined relative to the semiconductor operating layer.

2. The field effect transistor according to claim **1**, wherein said semiconductor operating layer includes a lower part semiconductor layer having an electrical conductivity type of a p type, a carrier drifting layer with un-doped formed on the lower part semiconductor layer, and a carrier supplying layer having a band gap energy larger than that of the carrier drifting layer, said recess part being formed by removing a part of the carrier drifting layer and the carrier supplying layer to a depth reaching the lower part semiconductor layer.

3. The field effect transistor according to claim **1**, wherein said semiconductor operating layer includes a contact region at a part contacting with the source electrode and the drain electrode.

4. The field effect transistor according to claim **1**, wherein said side wall has an angle of standing up greater than 30 degrees and smaller than 75 degrees.

5. The field effect transistor according to claim **4**, wherein said side wall has the angle of standing up smaller than 65 degrees.

6. A field effect transistor comprising:
- a substrate having an electrical conductivity type of an n type or a p type;
- a lower part semiconductor layer formed on the substrate, said lower part semiconductor layer having an electrical conductivity type the same as that of the substrate and a carrier density lower than that of the substrate;
- a semiconductor operating layer formed on the lower part semiconductor layer, said semiconductor operating layer including a side wall protruding from the lower part semiconductor layer in an inclined state, a carrier drifting layer having an electrical conductivity type opposite to that of the lower part semiconductor layer, and a carrier supplying layer having an electrical conductivity type the same as that of the lower part semiconductor layer;
- a source electrode formed on the semiconductor operating layer for connecting to the carrier drifting layer and the carrier supplying layer;
- a drain electrode formed on a rear surface of the substrate;
- a gate insulating layer formed over an upper portion of the semiconductor operating layer, the side wall, and an upper portion of the lower part semiconductor layer; and
- a gate electrode formed on the gate insulating layer for covering the side wall.

7. The field effect transistor according to claim **6**, wherein said side wall has an angle of standing up greater than 30 degrees and smaller than 75 degrees.

8. The field effect transistor according to claim **7**, wherein said side wall has the angle of standing up smaller than 65 degrees.

9. A method for manufacturing a field effect transistor formed of a nitride based compound semiconductor, comprising the steps of:
- forming a semiconductor operating layer on a substrate;
- forming a recess part at a part of the semiconductor operating layer, said recess part including a side wall inclined relative to the semiconductor operating layer;
- forming a source electrode and a drain electrode on the semiconductor operating layer with the recess part in between for electrically connecting to the semiconductor operating layer;